UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,346	03/16/2007	Akihiko Namba	050212-0716	3240

20277 7590 09/09/2008

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
09/09/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,346	NAMBA ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/27/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 – 11 and 13 – 15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: a second semiconductor layer, which is necessary for device operation and claimed properties.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 7, and 9 – 13 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over McClure et al. (US 2004/0149993 A1), with evidentiary support provided by Clevenger et al. (US 6,579,743 B2) and Davis et al. (US RE34,861).

a. Regarding claim 1, **McClure discloses a diamond n-type semiconductor** (e.g. figure 1) **comprising a first diamond semiconductor which has n-type conduction** (n-type silicon carbide layer 20, disclosed in ¶ [0010] – [0012] of McClure. Clevenger discloses that silicon carbide may be considered to be a "diamond" in col. 3, lines 18 – 21) **and in which a distortion or defect is artificially formed** (as disclosed in ¶ [0010] of McClure, the layer 20 is doped with dopants, and therefore a distortion may be formed in the lattice due to the impurity. Furthermore, the patentability of a product does not depend on the method of production. See MPEP 2113).

wherein in said first diamond semiconductor, a conductor exhibits an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more within a temperature region from 0°C to 300°C.

b. Claim 2, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein, in said first diamond semiconductor, the conductor exhibits a Hall coefficient positively correlated with temperature in a temperature range which has a width of 100°C or more and is included within a temperature region from 0°C to 300°C**

c. Claim 3, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein the temperature range included within the temperature region from 0°C to 300°C has a width of over 200°C or more**

d. Claim 4, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor has a resistivity of 500 Ωcm or less at a temperature within the temperature region from 0°C to 300°C**

e. Claim 5, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein the electron concentration of said first diamond semiconductor is always 10^{16} cm^{-3} or more in the temperature region from 0°C to 300°C.**

Regarding claims 1 – 5, the device of figure 1 contains an n-type diamond semiconductor layer (layer 20) containing a concentration phosphorus dopant, as disclosed in paragraphs [0010] – [0012], which resides on a silicon carbide layer (layer 12) as disclosed in paragraphs [0010] – [0012]. Since the device of McClure meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claims 1 - 5, are presumed inherent to the device of McClure. See MPEP 2112.01.

f. Regarding claim 6, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor contains more than 5 x 10^{19} cm^{-3} in total of at least one kind of donor element** (paragraph [0010] discloses a dopant concentration to be between 1 x 10^{19} cm^{-3} and 1 x 10^{21} cm^{-3}).

g. Regarding claim 7, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor contains at least P (phosphorus) as the donor element** (paragraph [0011] discloses the N-type dopants of layer 20 to be phosphorus).

h. Regarding claim 9, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor contains an impurity element other than a donor element together with the donor element** (as disclosed in ¶ [0010] – [0012], the first diamond semiconductor is made of silicon carbide, whereby the silicon in the carbon structure of silicon carbide may be considered to be an impurity element. The silicon carbide semiconductor layer 20 is further doped with phosphorus as the donor element).

i. Regarding claim 10, **McClure discloses a diamond n-type semiconductor according to claim 9, as cited above, wherein said first diamond semiconductor contains Si of 1 x 10^{17} cm^{-3} or more as the impurity element** (the first diamond semiconductor 20 is silicon carbide, which has a concentration of silicon of 2.4 x 10^{22} cm^{-3} (silicon carbide is 50% silicon and 50% carbide by molecular structure, the molar mass is 40.1 g/mol, and the density is 3.22 g/cm^3))

j. Regarding claim 11, **McClure discloses a diamond n-type semiconductor according to claim 1, as cited above, wherein said first diamond semiconductor is monocrystal diamond** (¶ [0011] discloses forming the first semiconductor by the process of US Patent RE 34,861, which describes forming single crystal silicon carbide layers (abstract and col. 4, lines 63 - 66 of RE 34,861)).

k. Regarding claim 12, **McClure discloses a diamond n-type semiconductor according to claim 1, further comprising a second diamond semiconductor provided adjacent to said first diamond semiconductor and turned out to be n-type** (second n-type silicon carbide layer 12, disclosed in ¶ [0010] – [0012] of McClure, is adjacent to the first n-type silicon carbide semiconductor layer 20. Clevenger discloses that silicon carbide may be considered to be a “diamond” in col. 3, lines 18 – 21),

wherein, in said second diamond semiconductor, a conductor exhibits an electron concentration not negatively correlated with temperature and a Hall coefficient not positively correlated with temperature (The device of figure 1 contains an n-type diamond semiconductor layer (layer 20) containing a concentration phosphorus dopant, as disclosed in paragraphs [0010] – [0012], which resides on a silicon carbide layer (layer 12) as disclosed in paragraphs [0010] – [0012]. Since the device of McClure meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration and Hall coefficient as claimed in claim 12, are presumed inherent to the device of McClure. See MPEP 2112.01).

l. Regarding claim 13, **McClure discloses a semiconductor device at least partly employing a diamond n- type semiconductor according to claim 1** (figure 1, using the invention of claim 1, as cited above, is a semiconductor device used to emit light as an LED (light emitting diode), as disclosed in ¶ [0010]).

5. Claim 15 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Yoshida (US 6,340,393 B1). **Yoshida discloses a method of manufacturing a diamond n-type semiconductor** (e.g. as seen in figure 3), **said method comprising the steps of:**

preparing a diamond substrate (substrate 2); **and**

epitaxially growing a diamond semiconductor on said diamond substrate while artificially introducing an impurity element other than a donor element to said diamond substrate (diamond semiconductor layer 3 is epitaxially formed on substrate 2 while introducing impurity element H and donor element P in the layer, as disclosed in col. 5, lines 42 - 60), **whereby said diamond semiconductor has n-type conduction** (e.g. as disclosed in col. 6, lines 19 – 20) **and has a distortion or defect which is artificially formed therein** (the layer 3 is doped with phosphorus and hydrogen impurities, as disclosed in col. 5, lines 60 - 61, and therefore a distortion may considered to be formed artificially in the lattice due to the additions of impurities),

wherein, in said diamond semiconductor, a conductor exhibits an electron concentration negatively correlated with temperature in a temperature range which has a width of 100°C or more and which is included within the temperature region from 0°C to 300°C (The method of figure 3 contains an n-type diamond semiconductor layer containing a concentration phosphorus dopant (layer 3), which resides on a diamond layer (layer 2). Since the device of Yoshida meets the structural limitations of the claimed invention of the Applicant, the properties of the applicant's invention, such as the temperature dependence of the electron concentration, are presumed inherent to the device of Yoshida. See MPEP 2112.01).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure in view of Ando et al. (JP 2001-007385). **McClure discloses the diamond n-type semiconductor according to claim 6, as cited above, but is silent with respect to said first diamond semiconductor contains at least S (sulfur) as the donor element. However, McClure discloses that the dopants for the n-type semiconductor may be N-type dopants** (¶ [0011]).

Ando discloses a diamond n-type semiconductor (e.g. figure 3c, with diamond semiconductor layer 7, disclosed in ¶ [0018]) **wherein a first diamond**

semiconductor contains at least S (sulfur) as the donor element (paragraph [0018] discloses the dopant of layer 7 to be sulfur, which forms an n-type layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the diamond layer of McClure such that the donor element is sulfur because it was well-known in the art that sulfur can be used as a dopant in n-type diamond semiconductor layers, as disclosed by Ando. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use sulfur as the donor element because it produces an n-type semiconductor, with properties that are well known and studied within the art.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure in view of Yoshida. **McClure discloses the diamond n-type semiconductor according to claim 1, as cited above, but is silent with respect to the device being used in at least an electron emitting part of an electron emitting device.**

Yoshida discloses that diamond semiconductor devices can be used as an electron emitter (col. 5, lines 18 – 19).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use the diamond semiconductor of McClure as an electron emitter since Yoshida discloses that such semiconductor devices can be used as electron emitters. One would be motivated to use the devices in such a manner since a low resistivity exists in such devices, creating an efficient electron emitter.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida as applied to claim 15 above, and further in view of Hasegawa et al. (US 2002/0127405). **Yoshida discloses a method of manufacturing a diamond n-type semiconductor according to claim 15, as cited above, but is silent with respect to Si being artificially introduced as the impurity element to said diamond substrate.**

Hasegawa discloses that silicon can be used as an impurity element when doping semiconductor diamond (paragraphs [0037] – [0038]).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the method of Yoshida, such that the impurity element such as silicon is added during the formation of the semiconductor, since Hasegawa discloses that silicon can be used to dope diamond. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use silicon as an impurity element since silicon was a commonly used element in the semiconductor industry and is readily available with well-known properties.

Response to Arguments

11. Applicant's arguments with respect to claims 1 - 16 have been considered but are moot in view of the new ground(s) of rejection. In the Applicants response filed on May 27, 2008 the Applicant argues that the prior art does not disclose or anticipate that the *electron concentration of the semiconductor is negatively correlated with temperature*.

Although the Applicant claims a property of the semiconductor structure such as "*an electron concentration negatively correlated with temperature in a temperature range*", the Applicant has not claimed a structure that exhibits such a property. Currently, the device of McClure and the method of Yoshida discloses the claimed structure and method, respectively, and it has been held that when the prior art anticipates or renders obvious the claimed invention, then the properties of the invention may be considered to be inherent to the claimed invention. See MPEP 2112.01: "*Where the claimed and prior art products are identical or substantially identical in structure or composition, or produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established.*"

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
September 2, 2008